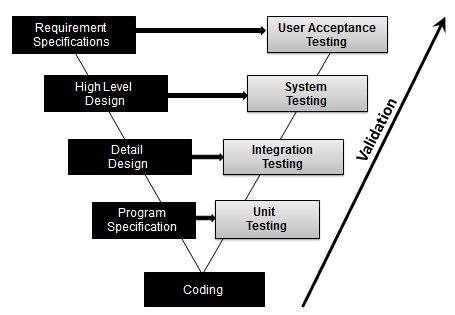
CHAPTER:1

## **Course Motivation and platform basic**

### **1.1 Introduction to testing and validation**

* The process of evaluating Product during the development process or at the end of the development process to determine whether it satisfies specified business requirements.
* Validation Testing ensures that the product actually meets the client's needs.



**fig-1:V-model represents validation**

## **1.2 Phases in Testing**



**Fig-2:phases of Testing**

## **1.2.1 Test Plan Types**

One can have the following types of test plans:

* **Master Test Plan:** A single high-level test plan for a project/product that unifies all other test plans.
* **Testing Level Specific Test Plans:** Plans for each level of testing.
  + Unit Test Plan
  + Integration Test Plan
  + System Test Plan
  + Acceptance Test Plan
* **Testing Type Specific Test Plans:**Plans for major types of testing like Performance Test Plan and Security Test Plan.

### **1.3 Below are the phases of STLC**

* Requirement Analysis
* Test Planning
* Test case development
* Test Environment setup
* Test Execution
* Test Cycle closure

## **1.4 Importance of testing**

Testing plays a vital role in development. In every company, testing is an important and valuable stage in the Development Life Cycle in order to:

**Improve Your Software**

The role of testing in software development begins with improved reliability, quality and performance of the software

**Quality assurance**

Quality plays a vital role in today’s competitive world

**Helps to avoid dangerous situations**

Without proper testing, produced software can be dangerous to the users

## **2.0 CISC and RISC**

### **2.1 What is The Difference Between RISC and CISC Architecture?**

The architecture of the Central Processing Unit (CPU) operates the capacity to function from “Instruction Set Architecture” to where it was designed. The architectural design of the CPU is Reduced instruction set computing (RISC) and Complex instruction set computing (CISC). CISC has the capacity to perform multi-step operations or addressing modes within one instruction set. It is the CPU design where one instruction works several low-level acts. For instance, memory storage, loading from memory, and an arithmetic operation. Reduced instruction set computing is a Central Processing Unit design strategy based on the vision that basic instruction set gives a great performance when combined with a microprocessor architecture which has the capacity to perform the instructions by using some microprocessor cycles per instruction. This article discusses the difference between the RISC and CISC architecture. The hardware part of the Intel is named as Complex Instruction Set Computer (CISC), and Apple hardware is Reduced Instruction Set Computer (RISC).

|  |  |
| --- | --- |
| **RISC** | **CISC** |
| 1. RISC stands for Reduced Instruction Set Computer. | 1. CISC stands for Complex Instruction Set Computer. |
| 2. RISC processors have simple instructions taking about one clock cycle. The average clock cycle per instruction (CPI) is 1.5 | 2. CSIC processor has complex instructions that take up multiple clocks for execution. The average clock cycle per instruction (CPI) is in the range of 2 and 15. |
| 3. Performance is optimized with more focus on software | 3. Performance is optimized with more focus on hardware. |
| 4. It has no memory unit and uses a separate hardware to implement instructions.. | 4. It has a memory unit to implement complex instructions. |
| 5. It has a hard-wired unit of programming. | 5. It has a microprogramming unit. |
| **6.**The instruction set is reduced i.e. it has only a few instructions in the instruction set. Many of these instructions are very primitive. | **6.**The instruction set has a variety of different instructions that can be used for complex operations. |
| **7.**The instruction set has a variety of different instructions that can be used for complex operations. | **7.**CISC has many different addressing modes and can thus be used to represent higher-level programming language statements more efficiently. |
| 8.Complex addressing modes are synthesized using the software. | 8.CISC already supports complex addressing modes |
| 9.Multiple register sets are present | 9.Only has a single register set |
| 10.RISC processors are highly pipelined | 10.They are normally not pipelined or less pipelined |
| 11. The complexity of RISC lies with the compiler that executes the program | 11. The complexity lies in the microprogram |
| 12. Execution time is very less | 12. Execution time is very high |
| 13. Code expansion can be a problem | 13. Code expansion is not a problem |
| 14. Decoding of instructions is simple. | 14. Decoding of instructions is complex |
| 15. It does not require external memory for calculations | 15. It requires external memory for calculations |
| 16. The most common RISC microprocessors are Alpha, ARC, ARM, AVR, MIPS, PA-RISC, PIC, Power Architecture, and SPARC. | 16. Examples of CISC processors are the System/360, VAX, PDP-11, Motorola 68000 family, AMD and Intel x86 CPUs. |

## **3.0 Intel Architecture (IA)**

Intel processors are designed in reference to 3 main abstract models

* + IA- 32 architecture
  + Intel 64 architecture
  + IA- 64 architecture

Intel compilers and libraries support three platforms: general combinations of processor architecture and operating system type. This section explains the terms that Intel uses to describe the platforms in its documentation, installation procedures and support site.

**IA-32 Architecture**refers to systems based on 32-bit processors generally compatible with the Intel Pentium® II processor, (for example, Intel Pentium® 4 processor or Intel Xeon® processor), or processors from other manufacturers supporting the same instruction set, running a 32-bit operating system.

**Intel 64 Architecture**refers to systems based on IA-32 architecture processors which have 64-bit architectural extensions, for example, Intel CoreTM2 processor family), running a 64-bit operating system such as Microsoft Windows XP\* Professional x64 Edition or Microsoft Windows Vista\* x64. If the system is running a 32-bit version of the Windows operating system, then IA-32 architecture applies instead. Systems based on AMD\* processors running a 64-bit version of Windows are also supported by Intel compilers for Intel 64 architecture applications.

**x-64** or IA32e is used as a short term for the 64 bit extensions of the "classical" x86 architecture; almost any "normal" PC produced in the last years have a processor based on such architecture.

**IA 64**  (also called **Intel Itanium architecture**) is the instruction set architecture (ISA) of the Itanium family of 64-bit [Intel](https://en.wikipedia.org/wiki/Intel) microprocessors. The IA-64 architecture receives the sigla EPIC, which means Explicit Parallel Instruction Computing. By using this sigla, Intel wants to say that the compiler will be the great responsible for determining and clearing the parallelism present in the instructions to be executed. This is a combination of concepts called speculation, predication and explicit parallelism. Next, we will briefly study each one of them.

## **3**.**1 INTEL 64 AND IA-32 PROCESSOR GENERATIONS**

**16-bit Processors and Segmentation (1978)**

The Intel 286 processor introduced protected mode operation into the IA-32 architecture. Protected mode uses the segment register content as selectors or pointers into descriptor tables. Descriptors provide 24-bit base addresses with a physical memory size of up to 16 MBytes, support for virtual memory management on a segment swapping basis, and a number of protection mechanisms. These mechanisms include:

• Segment limit checking

• Read-only and execute-only segment options

• Four privilege levels

**The Intel386 Processor (1985)**

The Intel386 processor was the first 32-bit processor in the IA-32 architecture family. It introduced 32-bit registers for use both to hold operands and for addressing. The lower half of each 32-bit Intel386 register retains the properties of the 16-bit registers of earlier generations, permitting backward compatibility. The processor also provides a virtual-8086 mode that allows for even greater efficiency when executing programs created for 8086/8088 processors. In addition, the Intel386 processor has support for: • A 32-bit address bus that supports up to 4-GBytes of physical memory

• A segmented-memory model and a flat memory model

• Paging, with a fixed 4-KByte page size providing a method for virtual memory management

• Support for parallel stages

**The Intel Pentium Processor (1993)**

The introduction of the Intel Pentium processor added a second execution pipeline to achieve superscalar performance (two pipelines, known as u and v, together can execute two instructions per clock). The on-chip first-level cache doubled, with 8 KBytes devoted to code and another 8 KBytes devoted to data. The data cache uses the MESI protocol to support more efficient write-back cache in addition to the write-through cache previously used by the Intel486 processor. Branch prediction with an on-chip branch table was added to increase performance in looping constructs. In addition, the processor added:

• Extensions to make the virtual-8086 mode more efficient and allow for 4-MByte as well as 4-KByte pages

• Internal data paths of 128 and 256 bits add speed to internal data transfers

• Burstable external data bus was increased to 64 bits

• An APIC to support systems with multiple processors

• A dual processor mode to support glueless two processor systems

A subsequent stepping of the Pentium family introduced Intel MMX technology (the Pentium Processor with MMX technology). Intel MMX technology uses the single-instruction, multiple-data (SIMD) execution model to perform parallel computations on packed integer data contained in 64-bit registers.

**The P6 Family of Processors (1995-1999)**

The P6 family of processors was based on a superscalar microarchitecture that set new performance standards; “P6 Family Microarchitecture.” One of the goals in the design of the P6 family microarchitecture was to exceed the performance of the Pentium processor significantly while using the same 0.6-micrometer, fourlayer, metal BICMOS manufacturing process. Members of this family include the following:

• **The Intel Pentium Pro** processor is three-way superscalar. Using parallel processing techniques, the processor is able on average to decode, dispatch, and complete execution of (retire) three instructions per clock cycle. The Pentium Pro introduced the dynamic execution (micro-data flow analysis, out-of-order execution, superior branch prediction, and speculative execution) in a superscalar implementation. The processor was further enhanced by its caches. It has the same two on-chip 8-KByte 1st-Level caches as the Pentium processor and an additional 256-KByte Level 2 cache in the same package as the processor.

• **The Intel Pentium II** processor added Intel MMX technology to the P6 family processors along with new packaging and several hardware enhancements. The processor core is packaged in the single edge contact cartridge (SECC). The Level l data and instruction caches were enlarged to 16 KBytes each, and Level 2 cache sizes of 256 KBytes, 512 KBytes, and 1 MByte are supported. A half-frequency backside bus connects the Level 2 cache to the processor. Multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep are supported to conserve power when idling.

• **The Pentium II Xeon** processor combined the premium characteristics of previous generations of Intel processors. This includes: 4-way, 8-way (and up) scalability and a 2 MByte 2nd-Level cache running on a full frequency backside bus.

• **The Intel Celeron processor** family focused on the value PC market segment. Its introduction offers an integrated 128 KBytes of Level 2 cache and a plastic pin grid array (P.P.G.A.) form factor to lower system design cost.

• **The Intel Pentium III** processor introduced the Streaming SIMD Extensions (SSE) to the IA-32 architecture. SSE extensions expand the SIMD execution model introduced with the Intel MMX technology by providing a Vol. 1 2-3 INTEL 64 AND IA-32 ARCHITECTURES new set of 128-bit registers and the ability to perform SIMD operations on packed single-precision floating point values.

• **The Pentium III Xeon** processor extended the performance levels of the IA-32 processors with the enhancement of a full-speed, on-die, and Advanced Transfer Cache.

**The Intel Core Duo and Intel Core Solo Processors (2006-2007)**

The Intel Core Duo processor offers power-efficient, dual-core performance with a low-power design that extends battery life. This family and the single-core Intel Core Solo processor offer microarchitectural enhancements over Pentium M processor family. Its enhanced microarchitecture includes

: • Intel Smart Cache which allows for efficient data sharing between two processor cores

• Improved decoding and SIMD execution

• Intel Dynamic Power Coordination and Enhanced Intel Deeper Sleep to reduce power consumption

• Intel Advanced Thermal Manager which features digital thermal sensor interfaces

• Support for power-optimized 667 MHz bus The dual-core Intel Xeon processor LV is based on the same microarchitecture as Intel Core Duo processor, and supports IA-32 architecture

**The Intel Atom Processor Family (2008)**

The first generation of Intel AtomTM processors are built on 45 nm process technology. They are based on a new microarchitecture, Intel AtomTM microarchitecture, which is optimized for ultra low power devices. The Intel AtomTM microarchitecture features two in-order execution pipelines that minimize power consumption, increase battery life, and enable ultra-small form factors. The initial Intel Atom Processor family and subsequent generations including Intel Atom processor D2000, N2000, E2000, Z2000, C1000 series provide the following features:

• Enhanced Intel SpeedStep Technology

• Intel Hyper-Threading Technology

• Deep Power Down Technology with Dynamic Cache Sizing

• Support for instruction set extensions up to and including Supplemental Streaming SIMD Extensions 3 (SSSE3).

• Support for Intel Virtualization Technology

• Support for Intel 64 Architecture (excluding Intel Atom processor Z5xx Series)

**2010 Intel Core Processor Family (2010)**

2010 Intel Core processor family spans Intel Core i7, i5 and i3 processors. They are based on Intel microarchitecture code name Westmere using 32 nm process technology. The innovative features can include:

• Deliver smart performance using Intel Hyper-Threading Technology plus Intel Turbo Boost Technology.

• Enhanced Intel Smart Cache and integrated memory controller.

• Intelligent power gating.

• Repartitioned platform with on-die integration of 45 nm integrated graphics.

• Range of instruction set support up to AESNI, PCLMULQDQ, SSE4.2 and SSE4.1.

**The Second Generation Intel Core Processor Family (2011)**

The Second Generation Intel Core processor family spans Intel Core i7, i5 and i3 processors based on the Sandy Bridge microarchitecture. They are built from 32 nm process technology and have innovative features including:

Intel Turbo Boost Technology for Intel Core i5 and i7 processors

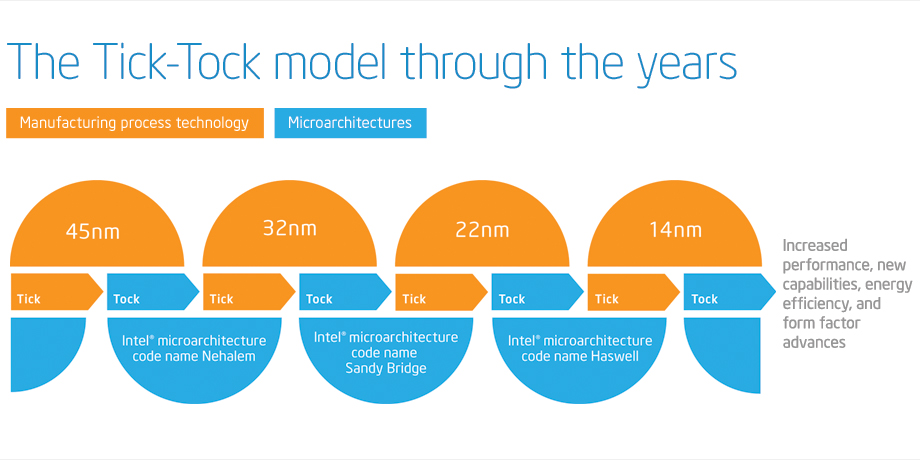
• Intel Hyper-Threading Technology

• Enhanced Intel Smart Cache and integrated memory controller.

• Processor graphics and built-in visual features like Intel Quick Sync Video, Intel InsiderTM etc.

• Range of instruction set support up to AVX, AESNI, PCLMULQDQ, SSE4.2 and SSE4.1

## **4.0 TICK\_TOCK**



**Tick-Tock** was an aggressive development model introduced by [Intel](https://en.wikichip.org/wiki/Intel) for their mainstream microprocessors in [2005](https://en.wikichip.org/wiki/2005) and phased out in [2016](https://en.wikichip.org/wiki/2016) whereby [microarchitecture](https://en.wikichip.org/wiki/intel/microarchitectures) changes were in-sync with their [process shrink](https://en.wikichip.org/wiki/process_shrink). Under the tick-tock scheme roughly every 12-18 months the Intel alternated between "Tick" and "Tock". Intel no longer uses this model, instead they use the [Process-Architecture-Optimization](https://en.wikichip.org/wiki/intel/process-architecture-optimization) (PAO).

Under the Tick-Tock Model:

* **Tick** - With each tick, Intel advances their manufacturing [process technology](https://en.wikichip.org/wiki/process_technology) in line with [Moore's Law](https://en.wikichip.org/wiki/Moore%27s_Law). Each new [process](https://en.wikichip.org/wiki/process_technology) introduces higher [transistor density](https://en.wikichip.org/wiki/transistor_density) and a generally a plethora of other advantages such as higher performance and lower power consumption. During a tick, Intel retrofits [their previous](https://en.wikichip.org/wiki/intel/microarchitectures) [microarchitecture](https://en.wikichip.org/wiki/microarchitecture) to the new process which inherently yielded better performance and energy saving. At this phase, only lightweight features and improvements are introduced.
* **Tock** - With each tock, Intel uses the their latest [manufacturing process technology](https://en.wikichip.org/wiki/manufacturing_process_technology) from their "tick" to manufacture a newly designed [microarchitecture](https://en.wikichip.org/wiki/microarchitecture). The new microarchitecture is designed with the new process in mind and typically introduces Intel's newest big features and functionalities. New [instructions](https://en.wikichip.org/w/index.php?title=instruction_set&action=edit&redlink=1) are often added during this cycle stage.

|  |  |  |  |
| --- | --- | --- | --- |
| **Intel Tick-Tock Roadmap** | | | |
| **Cycle** | [**Process**](https://en.wikichip.org/wiki/technology_node) | **Introduction** | **Micro­archi­tecture** |
| Tick | [65 nm](https://en.wikichip.org/wiki/65_nm) | 2005 | Pentium D |
| Tock | [65 nm](https://en.wikichip.org/wiki/65_nm) | 2006 | [Core](https://en.wikichip.org/wiki/intel/microarchitectures/core) |
| Tick | [45 nm](https://en.wikichip.org/wiki/45_nm) | 2007 | [Penryn](https://en.wikichip.org/wiki/intel/microarchitectures/penryn) |
| Tock | [45 nm](https://en.wikichip.org/wiki/45_nm) | 2008 | [Nehalem](https://en.wikichip.org/wiki/intel/microarchitectures/nehalem) |
| Tick | [32 nm](https://en.wikichip.org/wiki/32_nm) | 2009 | [Westmere](https://en.wikichip.org/wiki/intel/microarchitectures/westmere) |
| Tock | [32 nm](https://en.wikichip.org/wiki/32_nm) | 2010 | [Sandy Bridge](https://en.wikichip.org/wiki/intel/microarchitectures/sandy_bridge) |
| Tick | [22 nm](https://en.wikichip.org/wiki/22_nm) | 2011 | [Ivy Bridge](https://en.wikichip.org/wiki/intel/microarchitectures/ivy_bridge) |
| Tock | [22 nm](https://en.wikichip.org/wiki/22_nm) | 2013 | [Haswell](https://en.wikichip.org/wiki/intel/microarchitectures/haswell) |
| Tick | [14 nm](https://en.wikichip.org/wiki/14_nm) | 2014 | [Broadwell](https://en.wikichip.org/wiki/intel/microarchitectures/broadwell) |
| Tock | [14 nm](https://en.wikichip.org/wiki/14_nm) | 2015 | [Skylake](https://en.wikichip.org/wiki/intel/microarchitectures/skylake) |
|  |  |  |  |

## **5.0 PAO[Process Architecture optimization]**

**Process-Architecture-Optimization** was a temporary development model introduced by [Intel](https://en.wikichip.org/wiki/Intel) for their mainstream microprocessors in [2016](https://en.wikichip.org/wiki/2016) following the phase-out of their [Tick-Tock](https://en.wikichip.org/wiki/intel/tick-tock) model as a result of major delays and challenges involving their [10 nm process](https://en.wikichip.org/wiki/10_nm_process).

Under the Process-Architecture-Optimization Model:

* **Process** - With each process, Intel advances their manufacturing [process technology](https://en.wikichip.org/wiki/process_technology) in line with [Moore's Law](https://en.wikichip.org/wiki/Moore%27s_Law). Each new process introduces higher transistor density and generally a plethora of other advantages such as higher performance and lower power consumption. During a "process", Intel retrofits their [previous](https://en.wikichip.org/wiki/intel/microarchitectures) [microarchitecture](https://en.wikichip.org/wiki/microarchitecture) to the new process which inherently yields better performance and energy saving. During a "process", usually, just a few features and improvements are introduced.
* **Architecture** - With each architecture, Intel uses the their latest manufacturing [process technology](https://en.wikichip.org/wiki/process_technology) from their "process" to manufacture a newly designed [microarchitecture](https://en.wikichip.org/wiki/microarchitecture). The new microarchitecture is designed with the new process in mind and typically introduces Intel's newest big features and functionalities. New [instructions](https://en.wikichip.org/w/index.php?title=instruction_set&action=edit&redlink=1) are often added during this cycle stage.
* **Optimization** - With each optimization, Intel improves upon their [previous](https://en.wikichip.org/wiki/intel/microarchitectures) microarchitecture by introducing incremental improvements and enhancements without introducing any large charges. Additionally, the process itself enjoys various refinements as it matures. (For example with [Kaby Lake](https://en.wikichip.org/wiki/intel/microarchitectures/kaby_lake), an optimized process called "14 nm+" is used. The enhanced process had a number of transistor-level modifications done to it (e.g. taller fins) allowing for higher frequency at identical voltage levels.)

|  |  |  |  |
| --- | --- | --- | --- |
| **Intel PAO Roadmap** | | | |
| **Cycle** | [**Process**](https://en.wikichip.org/wiki/technology_node) | **Introduction** | **Micro­archi­tecture** |
| Process | [14 nm](https://en.wikichip.org/wiki/14_nm) | 2014 | [Broadwell](https://en.wikichip.org/wiki/intel/microarchitectures/broadwell) |
| Architecture | [14 nm](https://en.wikichip.org/wiki/14_nm) | 2015 | [Skylake (Client)](https://en.wikichip.org/wiki/intel/microarchitectures/skylake_(client)) |
| Optimization | [14 nm+](https://en.wikichip.org/wiki/14_nm) | 2016 | [Kaby Lake](https://en.wikichip.org/wiki/intel/microarchitectures/kaby_lake) |
| Optimization | [14 nm++](https://en.wikichip.org/wiki/14_nm) | 2017 | [Coffee Lake](https://en.wikichip.org/wiki/intel/microarchitectures/coffee_lake), [Skylake (Server)](https://en.wikichip.org/wiki/intel/microarchitectures/skylake_(server)) |
| Optimization | [14 nm++](https://en.wikichip.org/wiki/14_nm) | 2018 | [Whiskey Lake](https://en.wikichip.org/wiki/intel/microarchitectures/whiskey_lake) |
| Optimization | [14 nm++](https://en.wikichip.org/wiki/14_nm) | 2019 | [Cascade Lake](https://en.wikichip.org/wiki/intel/microarchitectures/cascade_lake), [Cooper Lake](https://en.wikichip.org/wiki/intel/microarchitectures/cooper_lake) |

## **6.0 PC AT/ATX**

The **IBM Personal Computer AT**, more commonly known as the **IBM AT** and also sometimes called the **PC AT** or **PC/AT**, was [IBM](https://en.wikipedia.org/wiki/IBM)'s second-generation [PC](https://en.wikipedia.org/wiki/IBM_Personal_Computer), designed around the 6 MHz [Intel 80286](https://en.wikipedia.org/wiki/Intel_80286) [microprocessor](https://en.wikipedia.org/wiki/Microprocessor) and released in 1984 as System Unit **5170**. The name **AT** stood for "Advanced Technology," and was chosen because the AT offered various technologies that were then new in personal computers; one such advancement was that the 80286 processor supported [protected mode](https://en.wikipedia.org/wiki/Protected_mode).

## **6.1 Power supply**

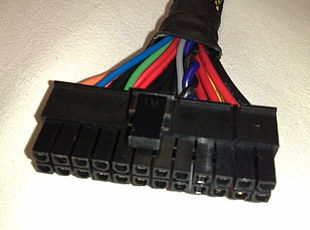
The IBM PC AT came with a 192-watt [switching power supply](https://en.wikipedia.org/wiki/Switching_power_supply). According to IBM's documentation, in order to function properly, the AT power supply needed a load of at least 7.0 amperes on the +5V line and a minimum of 2.5 amperes was on its +12V line. In practice, the AT power supply would randomly fail to start unless these minimum load requirements were met. Because the AT motherboard didn't provide much load on the +12V line, entry-level IBM AT models that didn't have a hard drive were shipped with a 5-ohm, 50-watt ([maximum power](https://en.wikipedia.org/wiki/Power_rating)) sandbar resistor connected on the +12V line of the hard disk power connector. In normal operation this resistor drew 2.4 amperes (28.8 watts), getting fairly hot.

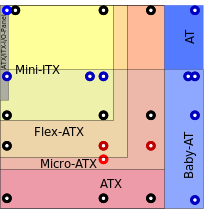
 **Fig-3:IBM PC AT (System Unit 5170)**

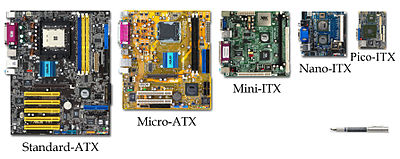
## **6.2 ATX**

**ATX** (**Advanced Technology eXtended**) is a motherboard and power supply configuration specification developed by [Intel](https://en.wikipedia.org/wiki/Intel) in 1995 to improve on previous [*de facto* standards](https://en.wikipedia.org/wiki/De_facto_standard) like the [AT design](https://en.wikipedia.org/wiki/AT_(form_factor)). It was the first major change in [desktop computer enclosure](https://en.wikipedia.org/wiki/Computer_case), [motherboard](https://en.wikipedia.org/wiki/Motherboard) and [power supply](https://en.wikipedia.org/wiki/Power_supply_unit_(computer)) design in many years, improving standardization and interchangeability of parts. The specification defines the key mechanical dimensions, mounting point, I/O panel, power and connector interfaces between a [computer case](https://en.wikipedia.org/wiki/Computer_case), a [motherboard](https://en.wikipedia.org/wiki/Motherboard) and a [power supply](https://en.wikipedia.org/wiki/Power_supply_unit_(computer)).

**fig-4: An ATX motherboard** 

 **fig-5 ATX 1.3v**



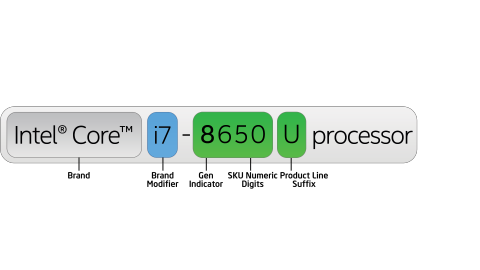
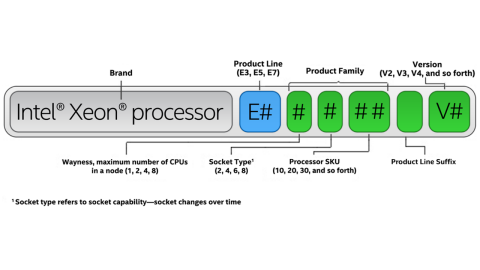


**Fig-6:Different motherboard form factors**

## **Size and Fit**

Both AT and ATX motherboards have been produced in various sizes throughout the years, and the form factors fit different computer cases depending on their size

## **Processor family7.0 Desktop and Mobile Processors**

****

**Fig-7:code names of desktop and processor**

| **Alpha Suffix** | **Description** | **Example** |
| --- | --- | --- |
| Desktop | | |
| K | Unlocked | Intel Core i9-9900K processor |
| F | Requires discrete graphics | Intel Core i9-9900KF processor |

| **Alpha Suffix** | **Description** | **Example** |
| --- | --- | --- |
| Desktop | | |
| K | Unlocked | 8th Gen Intel Core i7-8700K processor |
| Mobile | | |
| G | Includes discrete graphics on package | 8th Gen Intel Core i7-8705G processor |
| U | Ultra-low power | 8th Gen Intel Core i7-8650U processor |

| **Alpha Suffix** | | **Description** | **Example** |
| --- | --- | --- | --- |
| H | High performance graphics | | 7th Gen Intel Core™ i3-7100H processor |
| HK | High performance graphics, unlocked | | 7th Gen Intel Core™ i7-7820HK processor |
| HQ | High performance graphics, quad core | | 7th Gen Intel Core i7-7920HQ processor |
| U | Ultra-low power | | 7th Gen Intel Core i7-7500U processor |
| Y | Extremely low power | | 7th Gen Intel Core i7-7Y75 processor |

## **Comparing Mobile CPU vs Desktop CPU**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Type** | **Processor** | **Model** | **Cores** | **Clock Rate** | **GPU** | **GPU Clock** | **TDP** |
| Desktop | Intel Core i5 | 7500T | 4 | 2.7 GHz | HD 620 | 1100 MHz | 35W |
| Mobile | Intel Core i7 | 7500U | 2 | 2.7 GHz | HD 620 | 1050 MHz | 15W |

A desktop version will have a **higher speed processing and better cache** than a mobile CPU which will feature a reduced speed. Compare the two models below: the mobile core i7 CPU has the same clock rate as the Desktop i5 core. The Desktop has twice more cores than the mobile core i7 and a small improvement on the GPU Clock rated speed.

**Refer::** [**https://www.intel.in/content/www/in/en/processors/processor-numbers.html**](https://www.intel.in/content/www/in/en/processors/processor-numbers.html)

## **8.0 Intel families and generation**

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## **10.0 Xeon code names**

## 